

# ISO 11992-1:2003-04 (E)

## Road vehicles - Interchange of digital information on electrical connections between towing and towed vehicles - Part 1: Physical and data-link layer

---

| <b>Contents</b>           |   | <b>Page</b> |
|---------------------------|---|-------------|
| Foreword .....            |   | iv          |
| <b>1</b>                  | <b>Scope .....</b>  | <b>1</b>    |
| <b>2</b>                  | <b>Normative references .....</b>                         | <b>1</b>    |
| <b>3</b>                  | <b>Terms and definitions .....</b>                        | <b>2</b>    |
| <b>4</b>                  | <b>Abbreviations .....</b>                                | <b>2</b>    |
| <b>5</b>                  | <b>General specification .....</b>                        | <b>3</b>    |
| <b>6</b>                  | <b>Physical layer .....</b>                               | <b>3</b>    |
| 6.1                       | General requirements .....                                | 3           |
| 6.2                       | Physical media .....                                      | 3           |
| 6.3                       | Contacts .....  | 5           |
| 6.4                       | Physical medium attachment .....                          | 5           |
| 6.5                       | Physical signalling .....                                 | 12          |
| <b>7</b>                  | <b>Conformance test circuits .....</b>                    | <b>13</b>   |
| 7.1                       | General .....   | 13          |
| 7.2                       | Recessive output of the ECU .....                         | 13          |
| 7.3                       | Input resistance R1 .....                                 | 14          |
| 7.4                       | Dominant output of the ECU and serial resistance R2 ..... | 15          |
| 7.5                       | Receive threshold of recessive bits .....                 | 15          |
| 7.6                       | Receive threshold for dominant bit .....                  | 16          |
| 7.7                       | Offset voltage .....                                      | 16          |
| 7.8                       | Internal signal delay .....                               | 18          |
| 7.9                       | Bus failure management and power-on procedure .....       | 19          |
| 7.10                      | Bit timing .....  | 20          |
| <b>8</b>                  | <b>Data link layer .....</b>                              | <b>21</b>   |
| <b>9</b>                  | <b>Fault confinement .....</b>                            | <b>21</b>   |
| <b>Bibliography .....</b> |   | <b>22</b>   |